Proceso de Fabricación CMOS

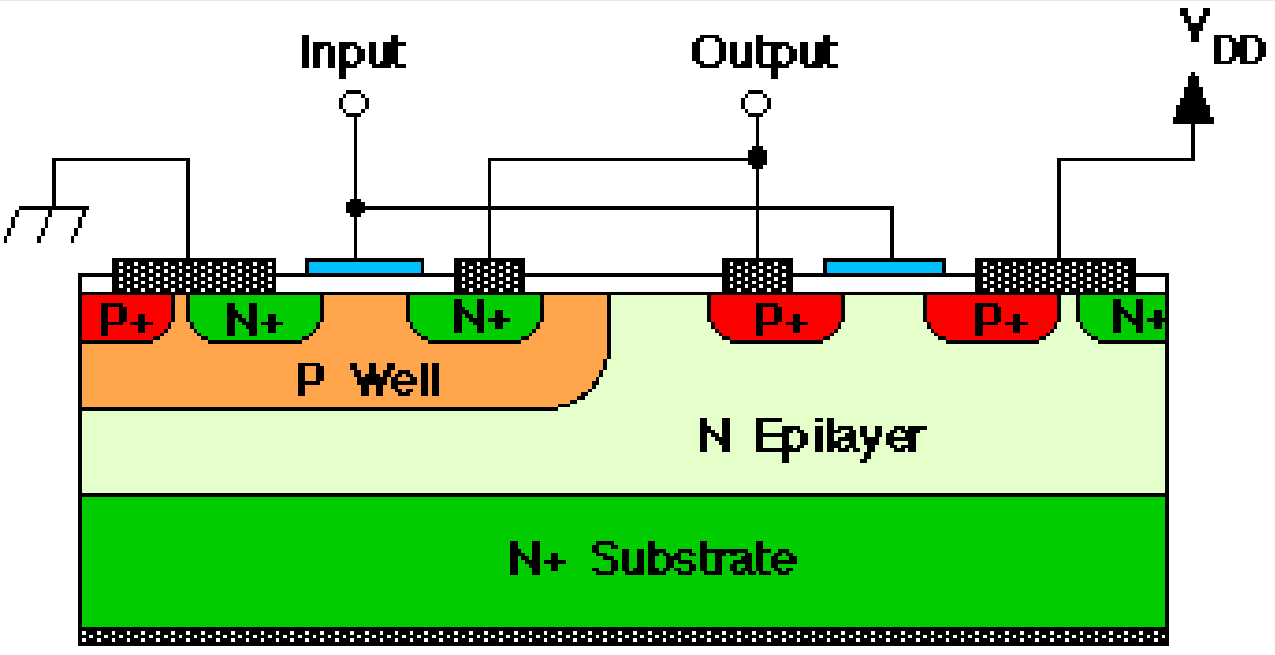
Asignatura: Tecnología de Computadores

Grupo: 22M

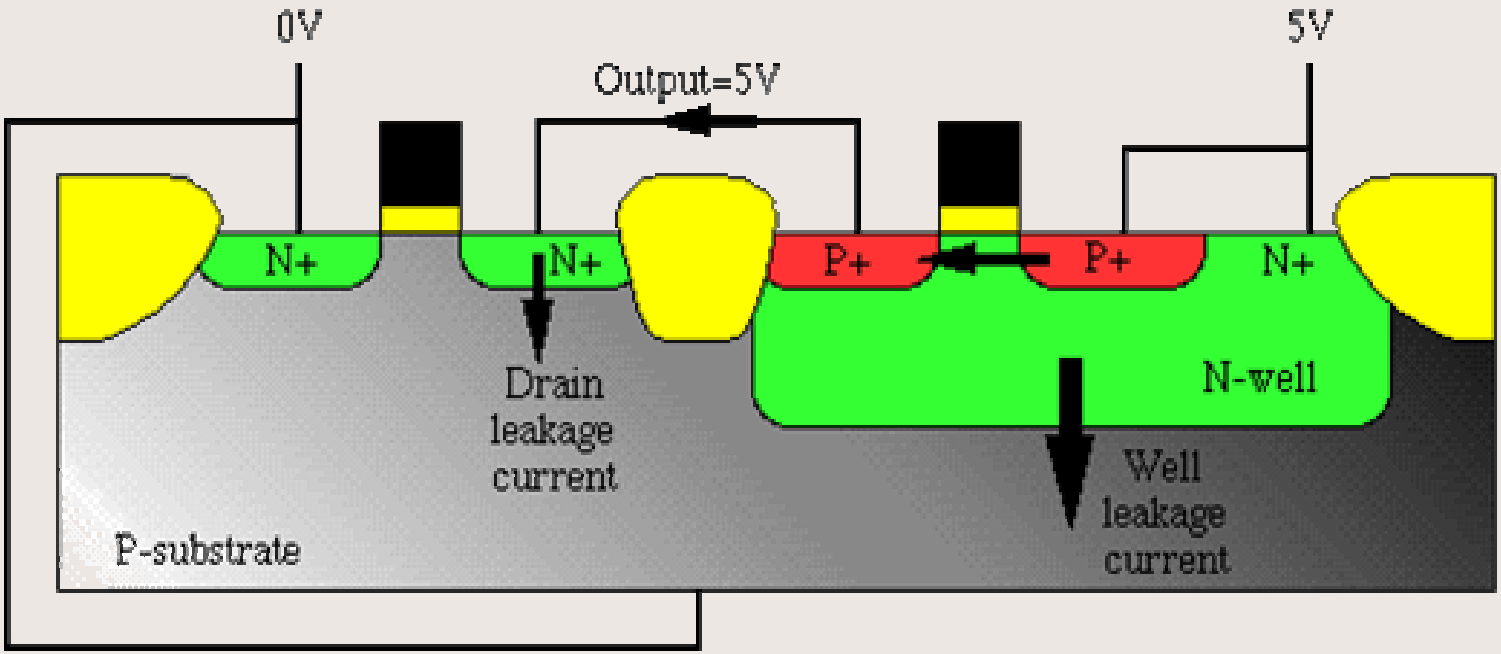
Curso 2004-2005

Procesos CMOS

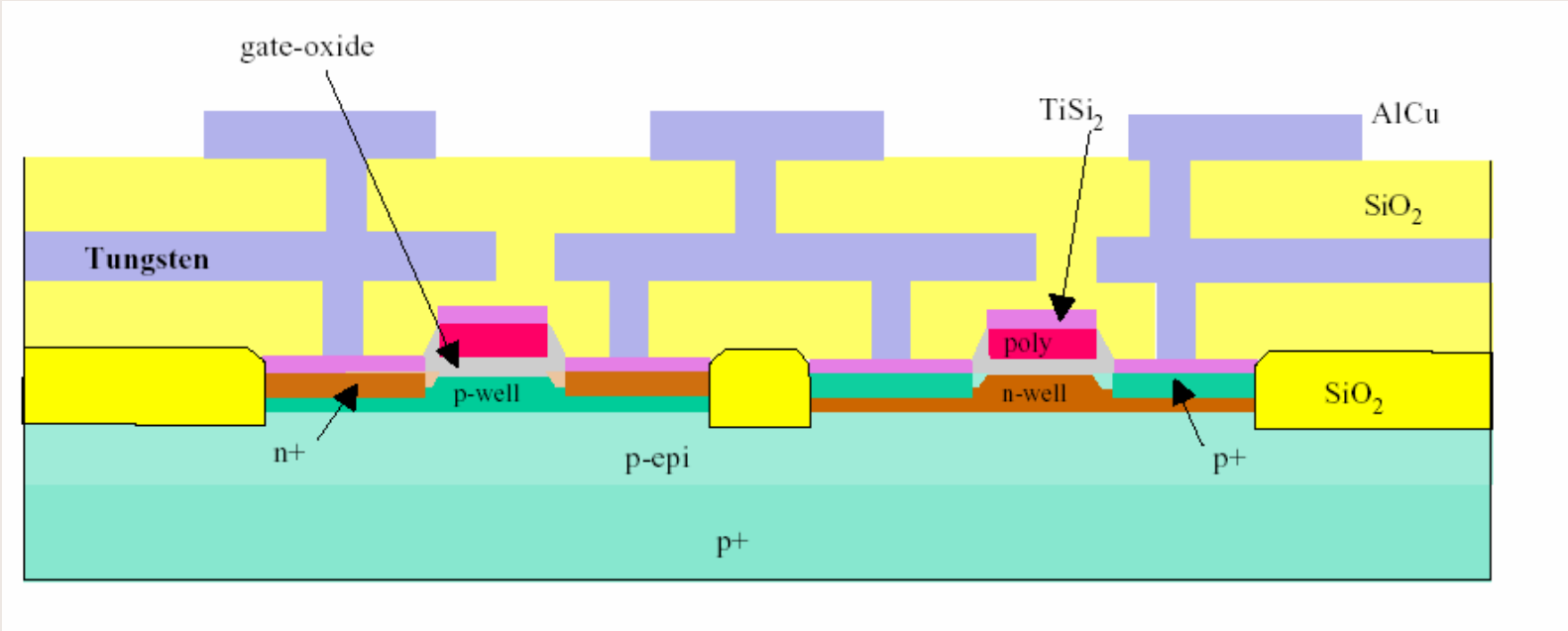
Procesos CMOS: pozo p



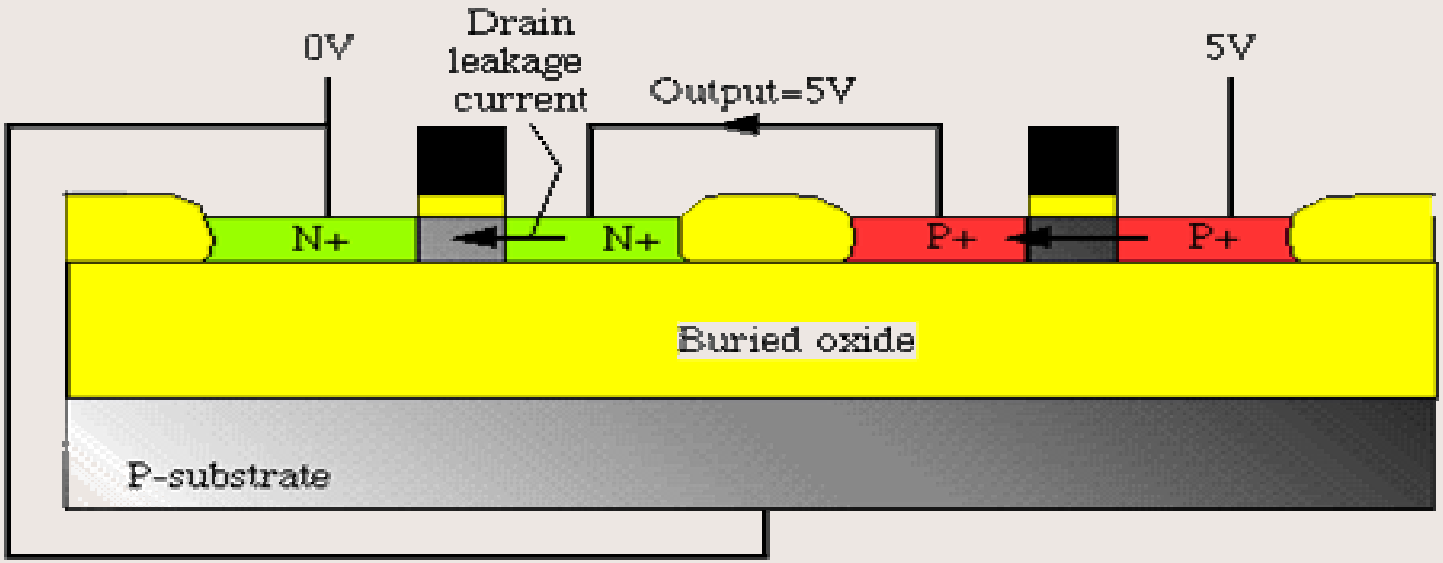
Procesos CMOS: pozo n



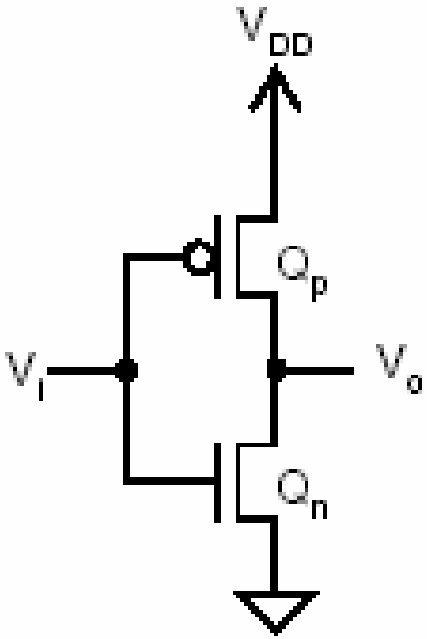
Procesos CMOS: doble pozo

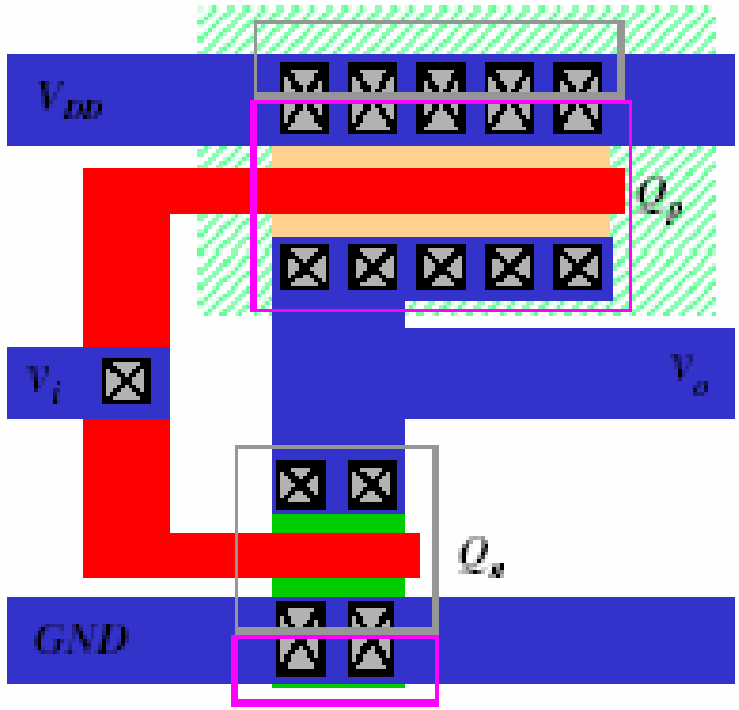


Procesos CMOS: SOI



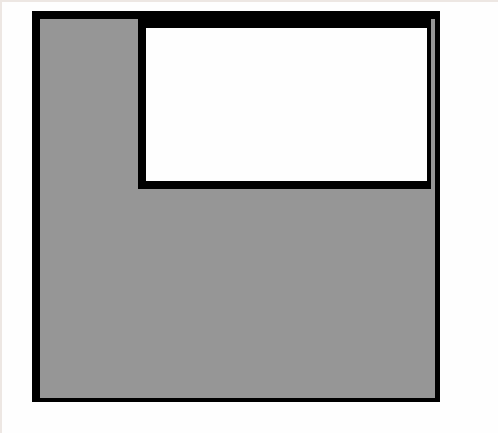
Layout de un inversor

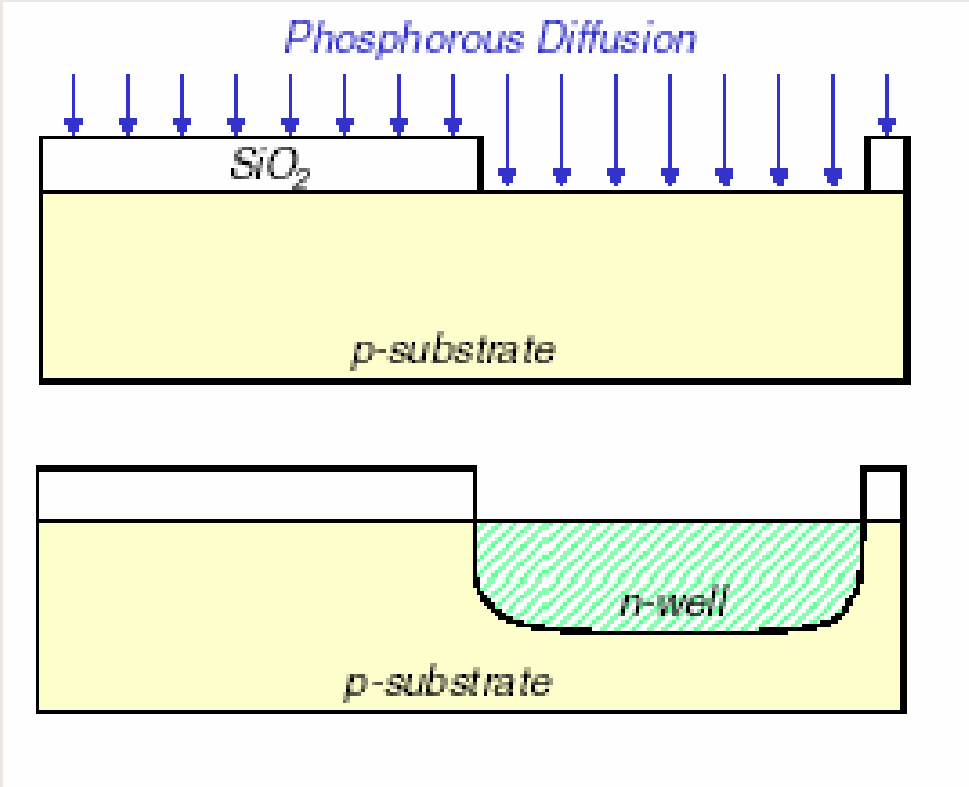




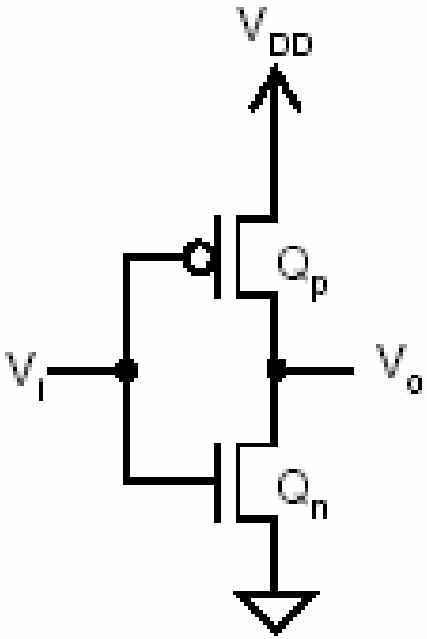
Mascára 1: Difusión pozo n

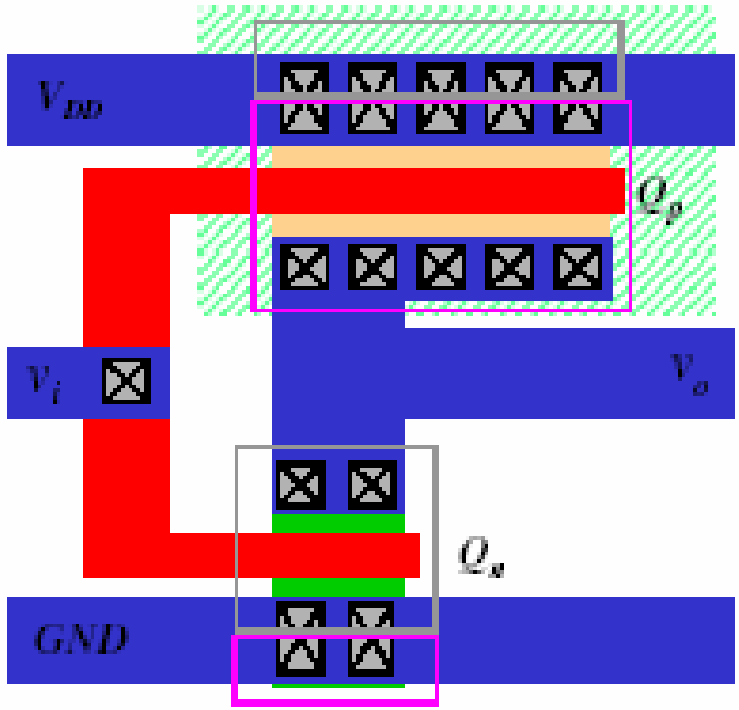
Mascara para eliminar SiO_2





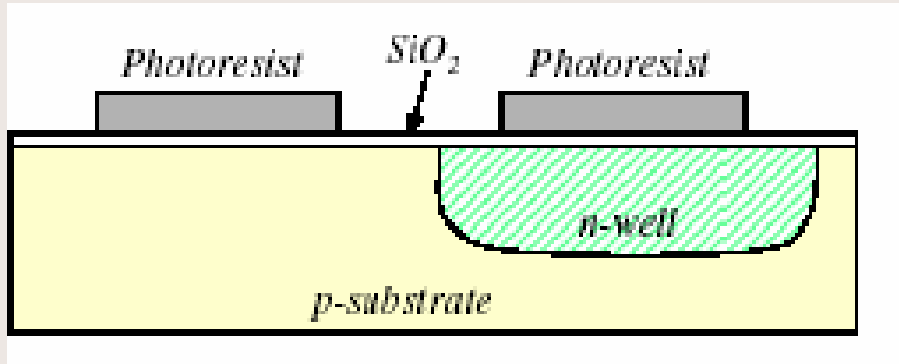
Layout de un inversor

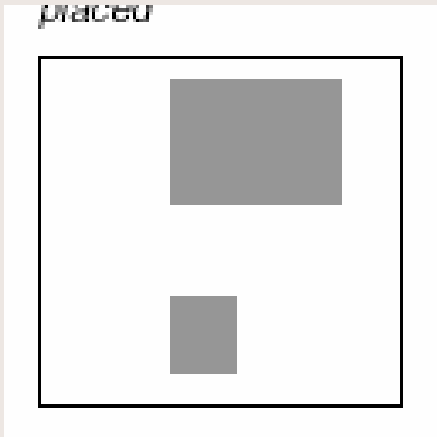


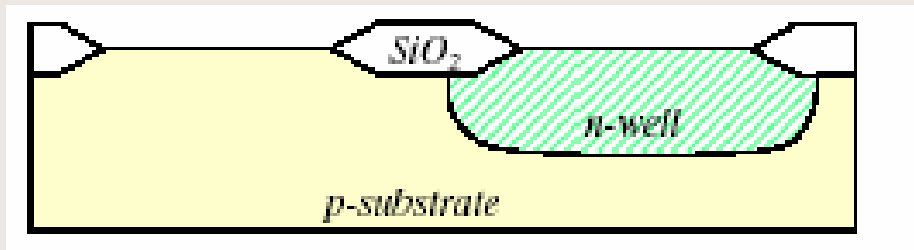


Máscara 2:Definición de regiones activas

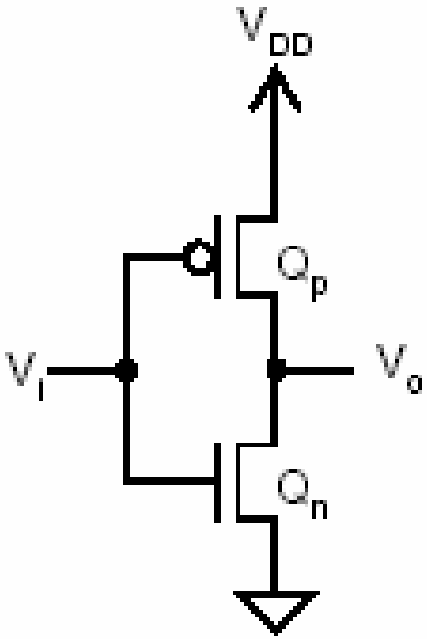
Define las regiones activas donde se van a colocar los dispositivos

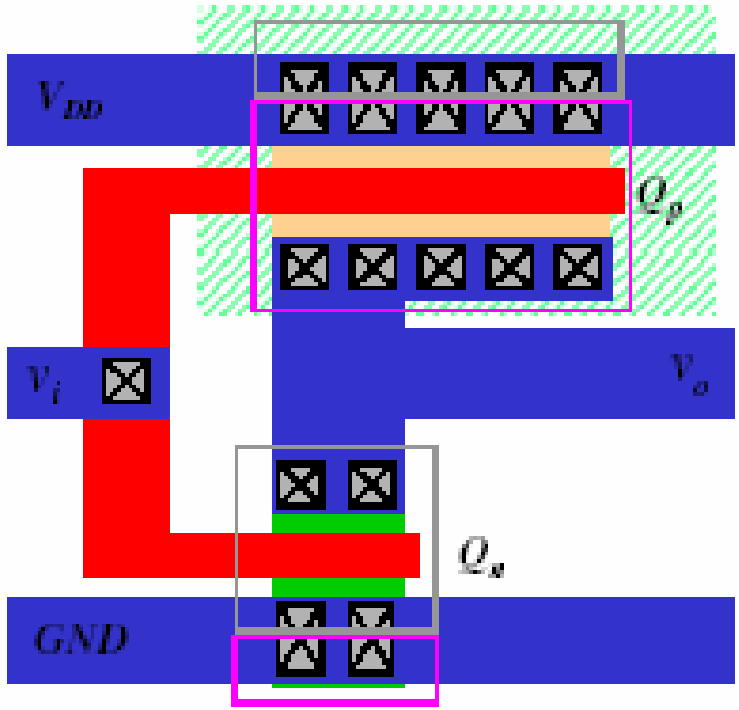






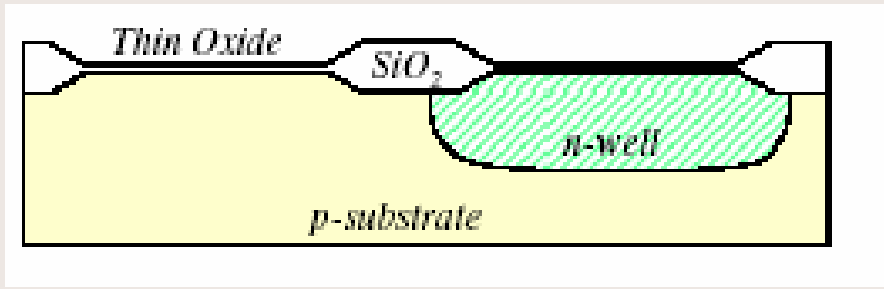
Layout de un inversor

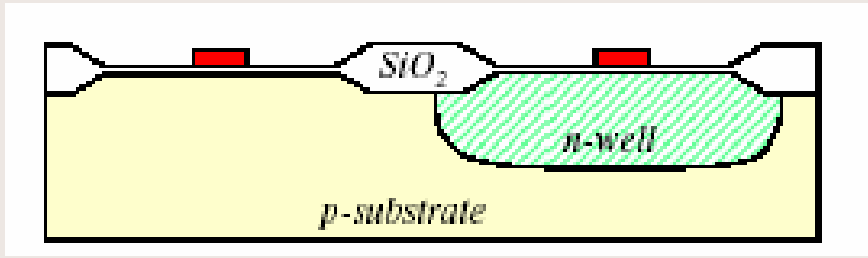


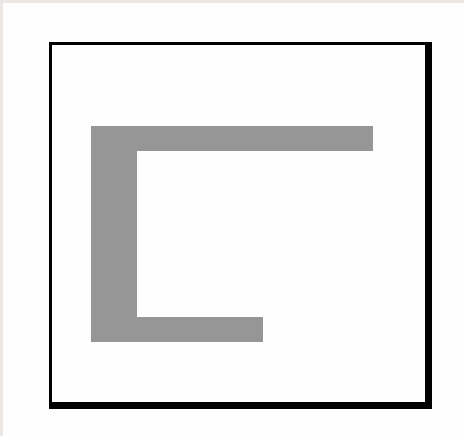


Máscara 3: Puerta de polisilicio

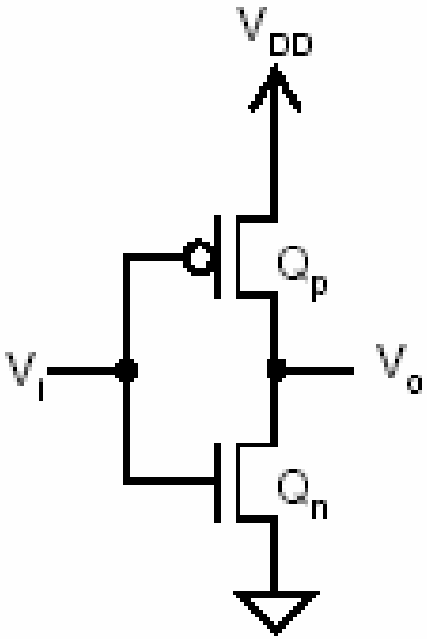
Se deposita el polisilicio de puerta

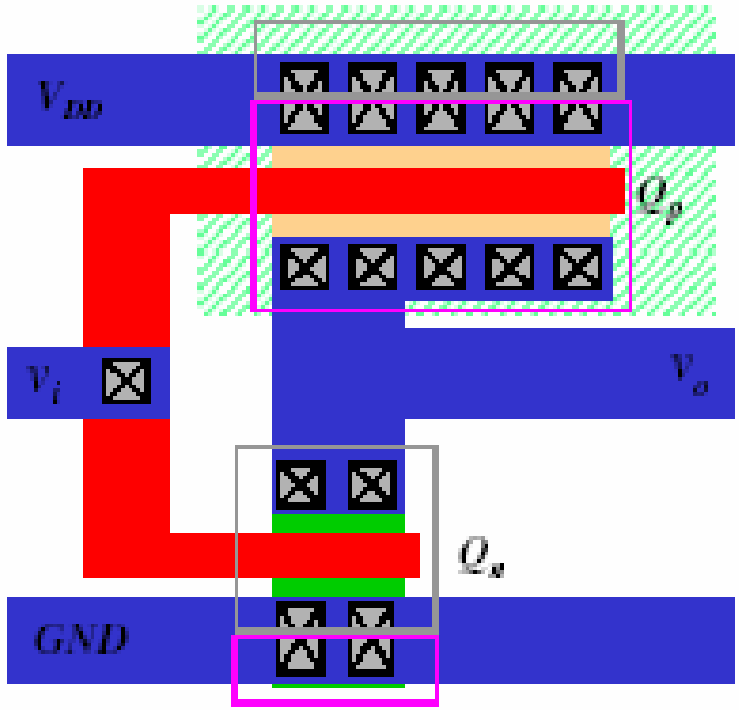






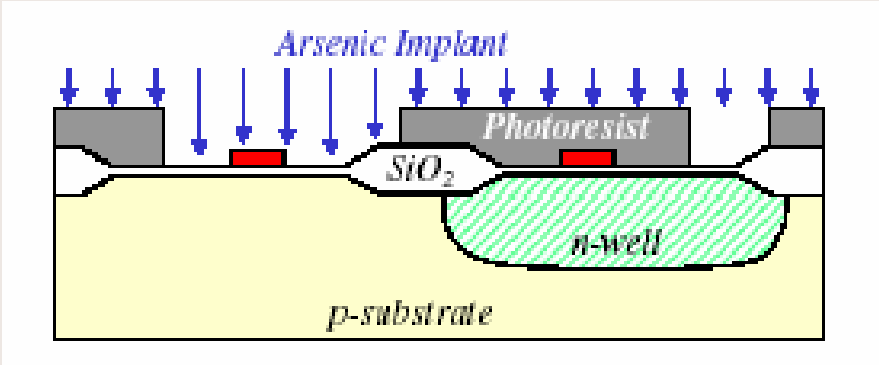
Layout de un inversor

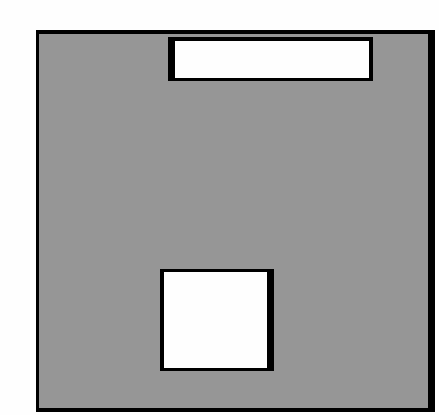


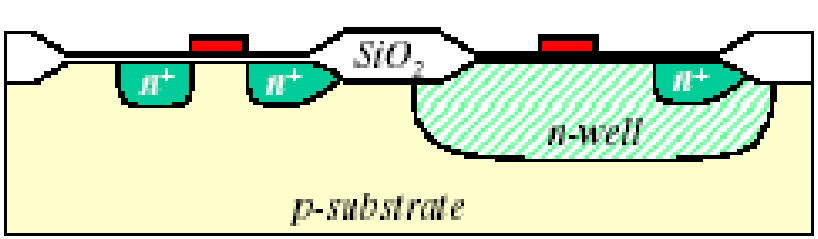


Máscara 4: Difusión n+

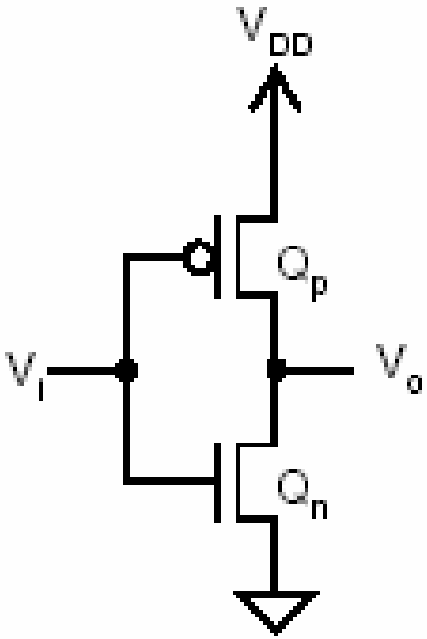
Se crea la fuente y el drenador de los dispositivos n

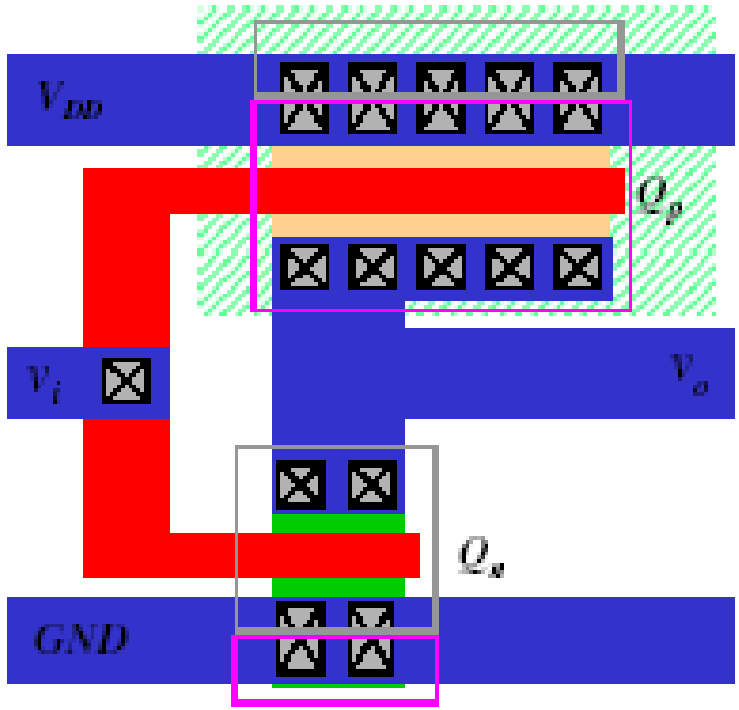






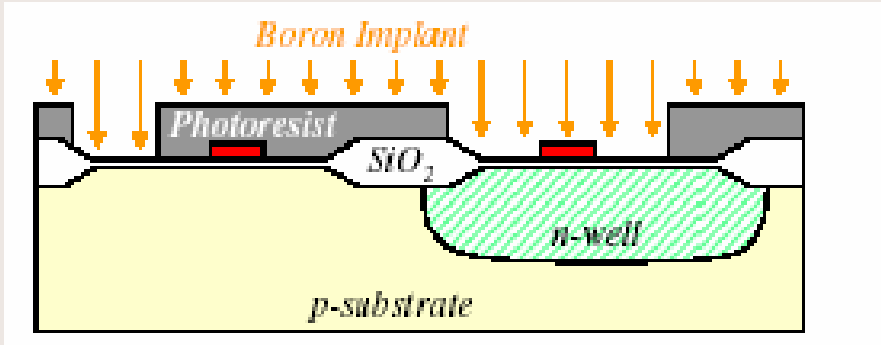
Layout de un inversor

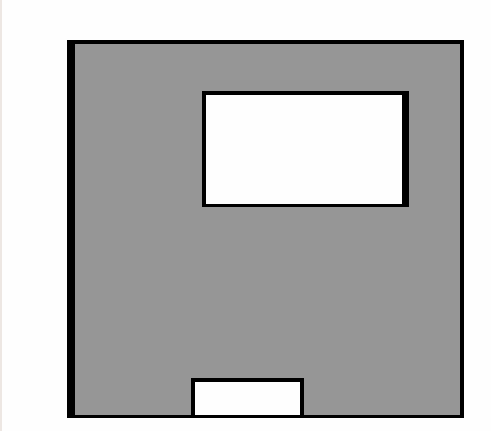


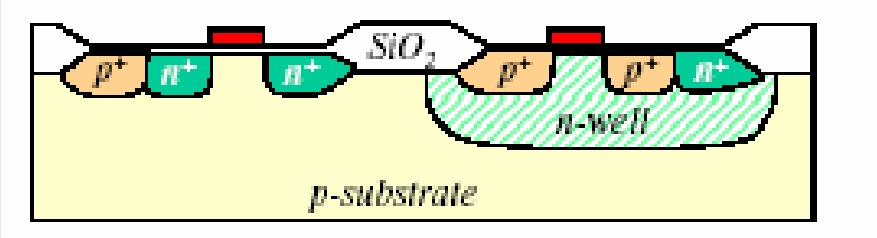


Máscara 5: Difusión p+

Se crea la fuente y el drenador de los dispositivos p

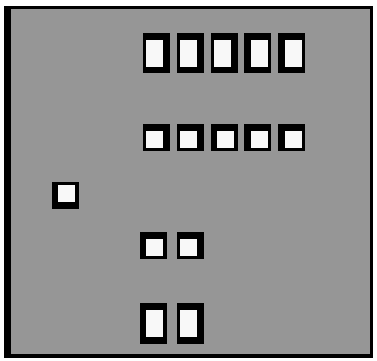


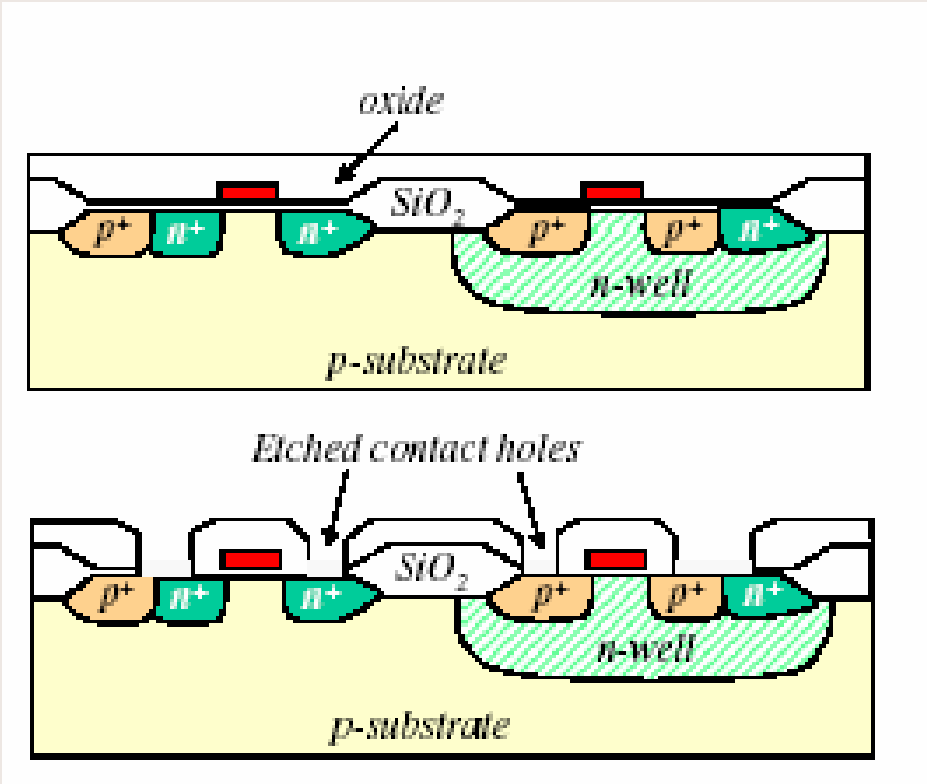




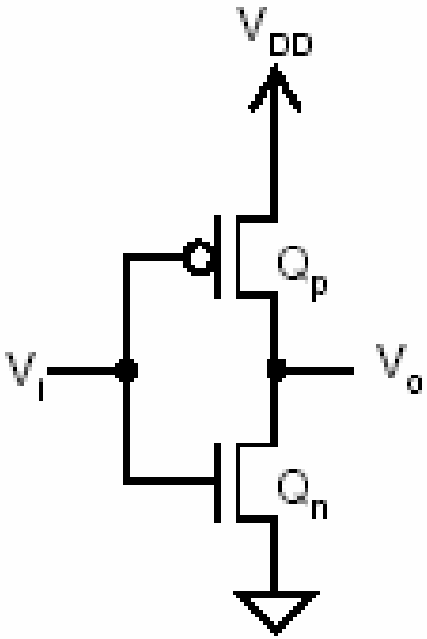
Máscara 6: Agujeros de contactos

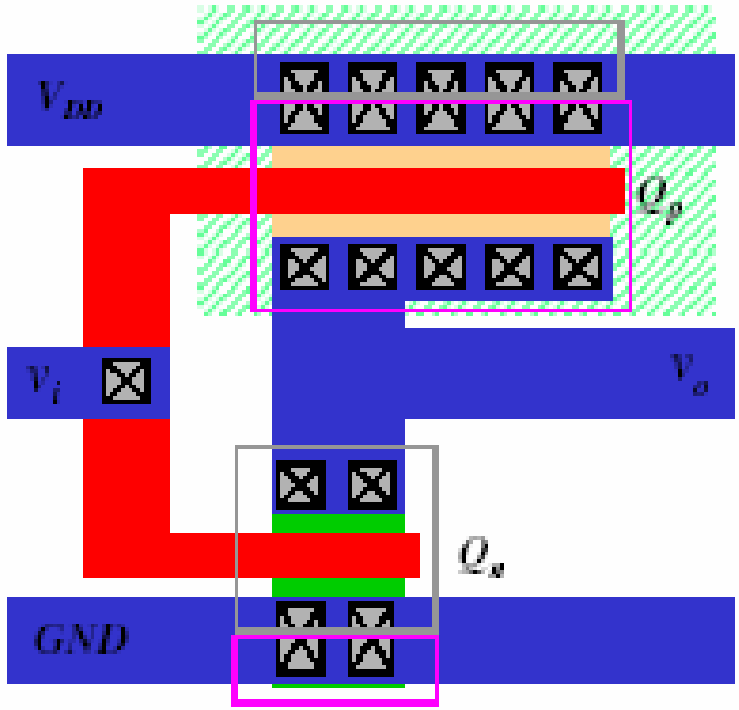
Determina las posiciones donde van los contactos





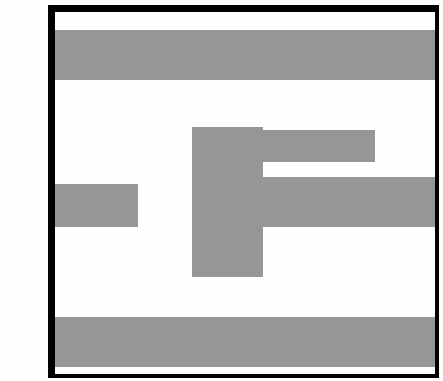
Layout de un inversor

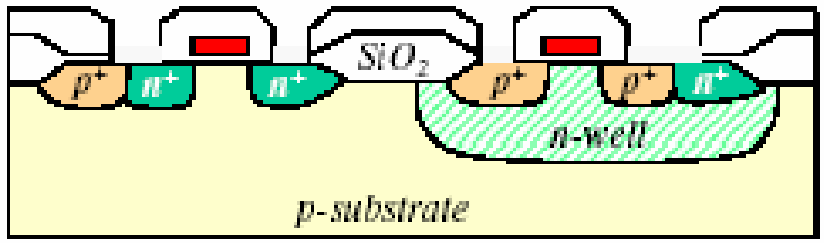


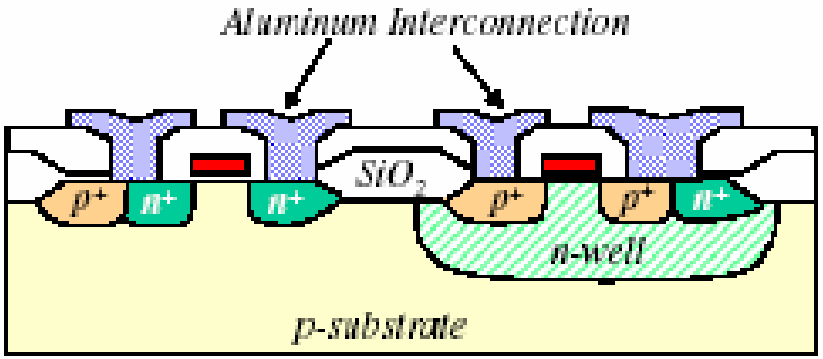


Máscara 7: Metalización

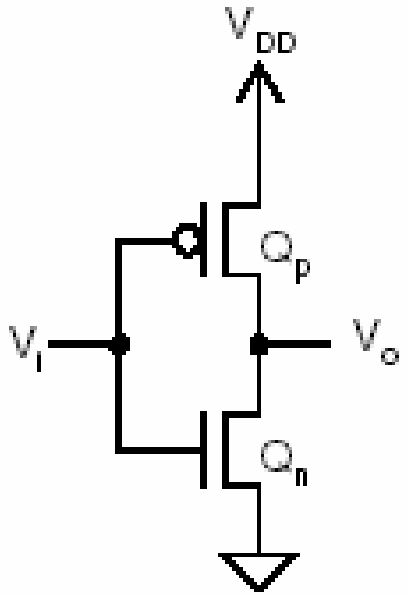
Determina las posiciones donde van las interconexiones

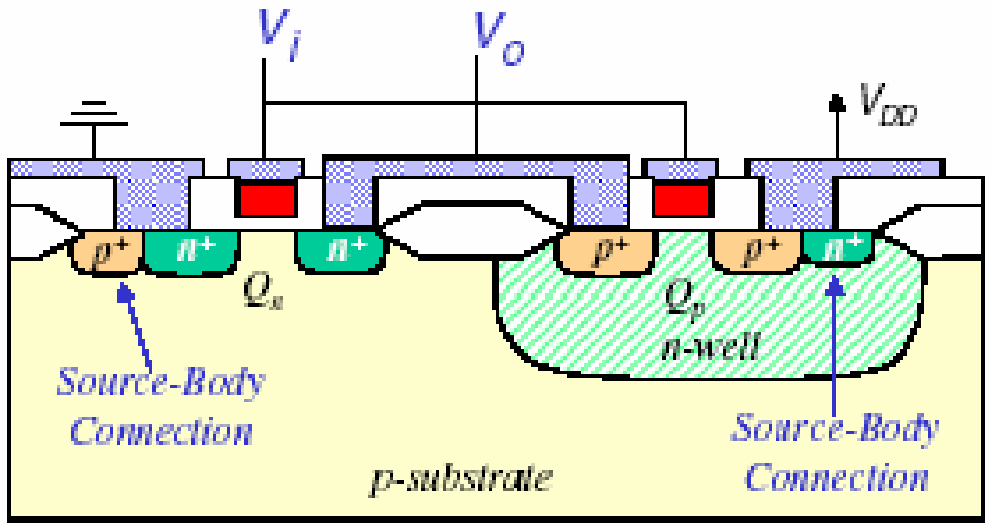




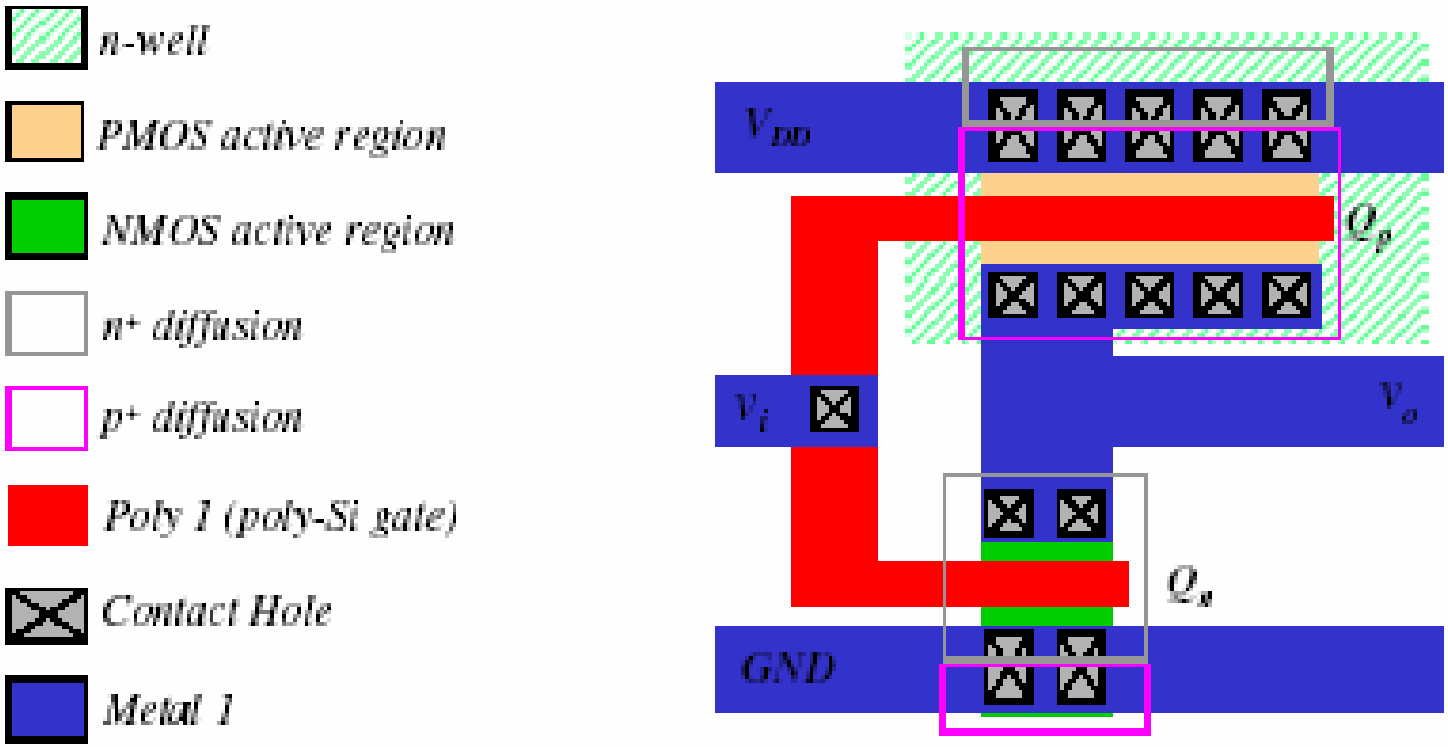


Sección de un inverso CMOS





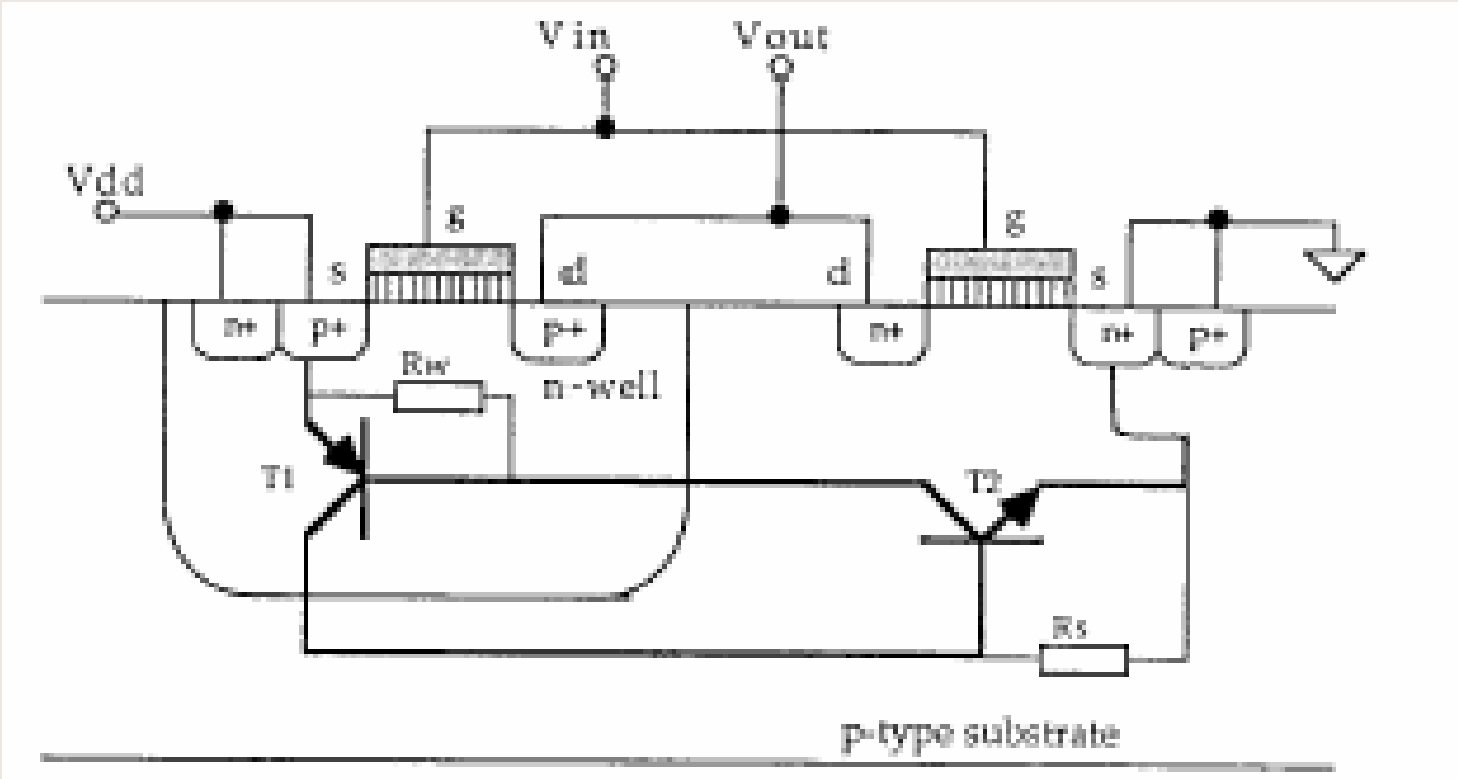
Layout de un inverso CMOS



Efecto latch-up

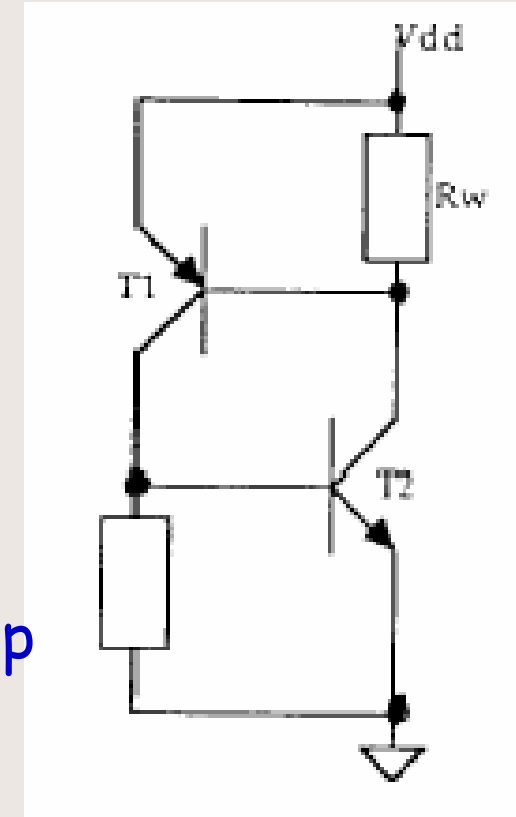
Definición: Generación de un camino de baja impedancia en CI CMOS entre alimentación y tierra debido a la aparición de transistores bipolares parásitos.

Efecto latch-up



Efecto latch-up

- T1 y T2 forman un circuito tristor
- Si Rw y/o Rs no 0 y T1 o T2 conducen, Vdd se cortocircuita con GND
- Los dos transistores conducen permanentemente hasta que se corta la alimentación → latch-up

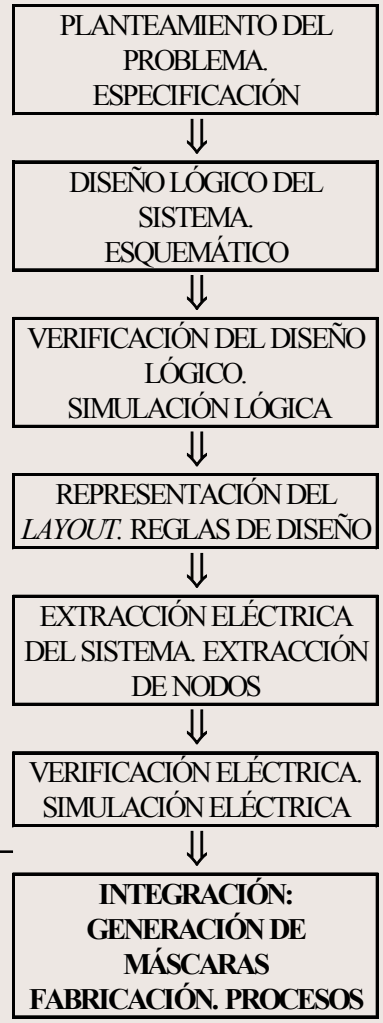


Reducción del efecto latch-up

- Reducción de la ganancia de los transistores parásitos
- Aumentando la distancia entre dispositivos de diferente tipo
- Anillos de guarda
- Contactos de pozo y substrato próximos a las fuentes de conexión

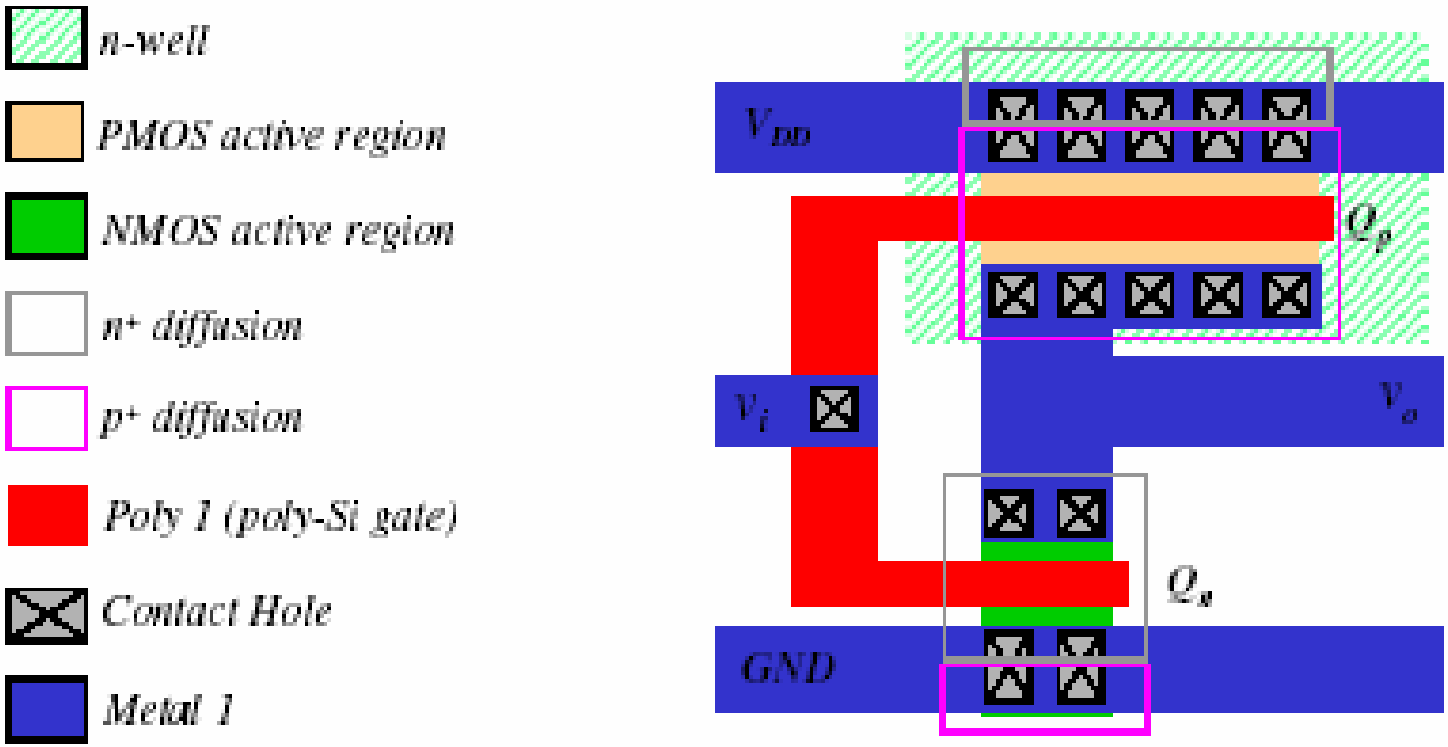
Realización de un CI

Proceso de diseño de un CI desde la concepción hasta la puesta en funcionamiento



(Caltech Interchange Format) Fichero C.I.F. ←

Layout de un inverso CMOS



- http://bwrc.eecs.berkeley.edu/Classes/icdesign/ee141_s02/Lectures/Lecture5-Manufacturing.pdf
- http://dunham.ee.washington.edu/ee539/notes/Chapter2.pdf
- http://tuttle.merc.iastate.edu/ee432/notes/mosprocessoverviews/cmos70/cmos70.htm

Sección de un transistor