CLC401
Fast Settling, Wideband High Gain Monolithic Op Amp

General Description
The CLC401 is a wideband, fast settling op amp designed for applications requiring gains greater than ±7. Constructed using an advanced complementary bipolar process and a proprietary design, the CLC401 features dynamic performance far beyond that of typical high speed monolithic op amps. For example, at a gain of +20, the −3dB bandwidth is 150MHz and the rise/fall time is only 2.5ns.

The wide bandwidth and linear phase (0.2˚ deviation from linear at 50MHz) and a very flat gain response makes the CLC401 ideal for many digital communication system applications. For example, demodulators need both DC coupling and high frequency amplification-requirements that are ordinarily difficult to meet.

The very fast 10ns settling to 0.1% and the ability to drive capacitive loads lend themselves well to flash A/D applications. Systems employing D/A converters also benefit from the settling time and also by the fact that current-to-voltage transimpedance amplification is easily accomplished.

The CLC401 provides a quick, effective design solution. Its stable operation over the entire ±7 to ±50 gain range prevents the need for external compensation. And, unlike many other high speed-op amps, the CLC401’s power dissipation of 150mW is compatible with designs which must limit total power dissipation or power supply requirements.

The CLC401 is based on National’s proprietary op amp topology that uses current feedback instead of the usual voltage feedback. This unique design has many advantages over conventional designs (such as settling time that is relatively independent of gain), yet it is used in basically the same way (see the gain equations in Figure 1 and Figure 2).

However, an understanding of the topology will aid in achieving the best performance. The discussion below will proceed for the non-inverting gain configuration with the inverting mode analysis being very similar.

Enhanced Solutions (Military/Aerospace)
SMD Number: 5962-89973

Features
- −3dB bandwidth of 150MHz
- 0.1% settling in 10ns
- Low power, 150mW
- Overload and short circuit protected
- Stable without compensation
- Recommended gain range, ±7 to ±50

Applications
- Flash, precision A/D conversion
- Photodiode, CCD preamps
- IF processors
- High speed modems, radios
- Line drivers
- DC coupled log amplifiers
- High speed communications

Connection Diagram

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Non-Inverting Frequency Response

Ordering Information

<table>
<thead>
<tr>
<th>Package</th>
<th>Temperature Range</th>
<th>Part Number</th>
<th>Package Marking</th>
<th>NSC Drawing</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-pin plastic DIP</td>
<td>−40˚C to +85˚C</td>
<td>CLC401AJP</td>
<td>CLC401AJP</td>
<td>N08E</td>
</tr>
<tr>
<td>8-pin plastic SOIC</td>
<td>−40˚C to +85˚C</td>
<td>CLC401AJE</td>
<td>CLC401AJE</td>
<td>M08A</td>
</tr>
</tbody>
</table>
### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Supply Voltage \( (V_{CC}) \): ±7V
- \( I_{OUT} \): 60mA
- Common Mode Input Voltage: ±\( V_{CC} \)
- Differential Input Voltage: 5V

### Operating Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ</th>
<th>Max/Min Ratings</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction Temperature Range</td>
<td>+150°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>−40°C to +85°C</td>
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</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Solder Duration (+300°C)</td>
<td>10 sec</td>
<td></td>
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</table>

### Electrical Characteristics

<table>
<thead>
<tr>
<th>Symbol Parameter</th>
<th>Conditions</th>
<th>Typ</th>
<th>Max/Min Ratings</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient Temperature</td>
<td>CLC401AJ</td>
<td>+25°C</td>
<td>−40°C</td>
<td>+25°C</td>
</tr>
</tbody>
</table>

#### Frequency Domain Response

- SSBW: −3dB Bandwidth
  \( V_{OUT} < 2V_{PP} \)
  - Typ: 150
  - Max/Min: 100 to 100
  - Ratings: 70 MHz
- LSBW: V OUT < 5V PP
  - Typ: 100
  - Max/Min: 65 to 65
  - Ratings: 55 MHz

#### Gain Flatness

- GFPL: Peaking
  - Condition: <25MHz
  - Typ: 0
  - Max/Min: <0.1 to <0.1
  - Ratings: dB
- GFPH: Peaking
  - Condition: >25MHz
  - Typ: 0
  - Max/Min: <0.2 to <0.2
  - Ratings: dB

#### Gain Rolloff

- GFR: Rolloff
  - Condition: <50MHz
  - Typ: 0.2
  - Max/Min: <1.0 to <1.0
  - Ratings: dB
  - DC to 50MHz: 0.2
  - Max/Min: <1.1 to <1.1
  - Ratings: deg

#### Linear Phase Deviation

- LPD: Linear Phase Deviation
  - DC to 50MHz: 0.2
  - Max/Min: <1.0 to <1.1
  - Ratings: deg

#### Time Domain Response

- TRS: Rise and Fall Time
  - 2V Step: 2.5
  - Max/Min: <3.5 to <3.5
  - Ratings: 5.0 ns
- TRL: 5V Step
  - 10
  - Max/Min: <15 to <15
  - Ratings: 15 ns
- TS: Settling Time to ±0.1%
  - 2V Step: 0
  - Max/Min: <10 to <10
  - Ratings: 10%
- OS: Overshoot
  - 2V Step: 1200
  - Max/Min: >800 to >800
  - Ratings: 700 V/µs

#### Distortion And Noise Response

- HD2: 2nd Harmonic Distortion
  - 2V PP, 20MHz: −45
  - Max/Min: −35 to −35
  - Ratings: −35 dBc
- HD3: 3rd Harmonic Distortion
  - 2V PP, 20MHz: −60
  - Max/Min: −50 to −50
  - Ratings: −45 dBc

#### Equivalent Input Noise

- SNF: Noise Floor
  - >1MHz: −158
  - Max/Min: −155 to −155
  - Ratings: −154 dBm (1Hz)
- INV: Integrated Noise
  - 1MHz to 150MHz: 35
  - Max/Min: <50 to <55
  - Ratings: μV

#### Static, DC Performance

<table>
<thead>
<tr>
<th>Symbol Parameter</th>
<th>Conditions</th>
<th>Typ</th>
<th>Max/Min Ratings</th>
<th>Units</th>
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<tbody>
<tr>
<td>VIO: Input Offset Voltage (Note 3)</td>
<td>3</td>
<td>±10.0</td>
<td>±6.0</td>
<td>±11.0</td>
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<tr>
<td>DVIO: Average Temperature Coefficient</td>
<td>20</td>
<td>±50</td>
<td>–</td>
<td>±50</td>
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<tr>
<td>IBIN: Input Bias Current (Note 3)</td>
<td>10</td>
<td>±36</td>
<td>±20</td>
<td>±20</td>
</tr>
<tr>
<td>DIBN: Average Temperature Coefficient</td>
<td>100</td>
<td>±200</td>
<td>–</td>
<td>±100</td>
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<tr>
<td>IBI: Input Bias Current (Note 3)</td>
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<td>46</td>
<td>30</td>
<td>40</td>
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<tr>
<td>DIBI: Average Temperature Coefficient</td>
<td>100</td>
<td>±200</td>
<td>–</td>
<td>±100</td>
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<tr>
<td>PSRR: Power Supply Rejection Ratio</td>
<td>55</td>
<td>50</td>
<td>50</td>
<td>50</td>
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<tr>
<td>CMRR: Common Mode Rejection Ratio</td>
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<td>50</td>
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<tr>
<td>ICC: Supply Current (Note 3)</td>
<td>No Load</td>
<td>15</td>
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#### Miscellaneous Performance

<table>
<thead>
<tr>
<th>Symbol Parameter</th>
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<th>Resistance</th>
<th>Typ</th>
<th>Max/Min Ratings</th>
<th>Units</th>
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<tbody>
<tr>
<td>RIN: Non-Inverting Input Resistance</td>
<td>200</td>
<td>&gt;50</td>
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<td>&gt;100</td>
<td>kΩ</td>
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<td>CIN: Capacitance</td>
<td>0.5</td>
<td>&lt;2.5</td>
<td>&lt;2.5</td>
<td>&lt;2.5</td>
<td>pF</td>
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</table>
**Electrical Characteristics** (Continued)

(A_{v} = +20, V_{CC} = ±5V, R_{L} = 100Ω, R_{i} = 1.5kΩ; unless specified).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ</th>
<th>Max/Min Ratings (Note 2)</th>
<th>Units</th>
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<tr>
<td>RO</td>
<td>Output Impedance</td>
<td>at DC</td>
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<td>&lt;0.3</td>
<td>Ω</td>
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<td></td>
<td></td>
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<td>&lt;0.3</td>
<td>&lt;0.3</td>
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<td></td>
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<td>&lt;0.3</td>
<td>&lt;0.3</td>
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<tr>
<td>VO</td>
<td>Output Voltage Range</td>
<td>No Load</td>
<td>3.5</td>
<td>&gt;3.0</td>
<td>V</td>
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<td>&gt;3.2</td>
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<td></td>
<td></td>
<td>&gt;3.2</td>
<td>&gt;3.2</td>
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<tr>
<td>CMIR</td>
<td>Common Mode Input Range</td>
<td>For Rated Performance</td>
<td>2.8</td>
<td>&gt;2.0</td>
<td>V</td>
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<td>&gt;2.5</td>
<td>&gt;2.5</td>
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<tr>
<td>IO</td>
<td>Output Current</td>
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<td>60</td>
<td>&gt;35</td>
<td>mA</td>
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<td>&gt;35</td>
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<td>&gt;50</td>
<td>&gt;50</td>
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</tbody>
</table>

**Note 1:** “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.

**Note 2:** Max/min ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

**Note 3:** AJ-level: spec. is 100% tested at +25°C.
Typical Performance Characteristics 

(T_A = 25˚, A_V = +20, V_CC = ±5V, R_L = 100Ω: Unless Specified).

Non-Inverting Frequency Response

Inverting Frequency Response

Frequency Response for Various R_Ls

Open-Loop Transimpedance Gain, Z(s)

2nd and 3rd Harmonic Distortion

2-Tone, 3rd Order, Intermodulation Intercept

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Typical Performance Characteristics (\(T_A = 25^\circ\), \(A_V = 20\), \(V_{CC} = \pm 5\) V, \(R_L = 100\Omega\): Unless Specified). (Continued)

**Equivalent Input Noise**

- Inverting Current: 17 pA/\(\sqrt{\text{Hz}}\)
- Non-Inverting Current: 2.6 pA/\(\sqrt{\text{Hz}}\)
- Voltage: 2.4 nV/\(\sqrt{\text{Hz}}\)

**CMRR and PSRR**

**Pulse Response**

- \(A_V = +20\)
- \(A_V = -20\)

**Settling Time**

- \(A_V = +20\)
- \(R_L = 100\)
- 2V output step

**Long-Term Settling Time**

\(A_V = +20\)

**Settling Time vs. Load Capacitance**

See recommended \(R_S\) versus Load Capacitance plot.
Typical Performance Characteristics (T_A = 25˚, A_V = +20, V_CC = ±5V, R_L = 100Ω: Unless Specified). (Continued)

Recommended R_S vs. Load Capacitance

![Graph showing Recommended R_S vs. Load Capacitance]

Low Gain & Transimpedance Applications

The CLC401 may be used at gains down to unity (A_V = ±1) by choosing R_f according to Equation (4) in this datasheet. The curves to the right show performance at inverting unity gain with R_f = 2500Ω, a configuration appropriate for D/A converter buffering and other transimpedance applications.

Frequency Response, A_V = −1, R_f = 2.25kΩ

![Graph showing Frequency Response]

Magnitude 1 dB/div

Phase 4.5°/div

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Equation 1

\[ \frac{V_O}{V_i} = 1 + \frac{R_f}{R_g} \]

where \( LG \) is the loop gain defined by,

Equation 2

\[ LG = \frac{Z(s)}{R_f} \times \frac{1}{1 + \frac{Z_i}{(R_f + R_g)}} \]

Equation 1 has a form identical to that for a voltage feedback amplifier with the differences occurring in the \( LG \) expression. For an idealized treatment, set \( Z_i = 0 \) which results in a very simple \( LG = Z(s)/R_f \). Derivation of the transfer function for the case where \( Z_i = 0 \) is given in Application Note AN300-1. Using the \( Z(s) \) (open-loop transimpedance gain) plot shown on the previous page and dividing by the recommended \( R_f = 1.5k \Omega \), yields a large loop gain at DC. As a result, Equation 1 shows that the closed-loop gain at DC is very close to \((1+R_f/R_g)\).

At higher frequencies, the roll-off of \( Z(s) \) determines the closed-loop frequency response which, ideally, is dependent only on \( R_f \). The specifications reported on the previous pages are therefore valid only for the specified \( R = 1.5k \Omega \). Increasing \( R \) from 1.5k\( \Omega \) will decrease the loop gain and bandwidth, while decreasing it will increase the loop gain possibly leading to inadequate phase margin and closed-loop peaking. Conversely, fixing \( R_f \) will hold the frequency response constant while the closed-loop gain can be adjusted using \( R_g \).

The CLC401 departs from this idealized analysis to the extent that the inverting input impedance is finite. With the low quiescent power of the CLC401, \( Z \approx 50 \Omega \) leading to drop in loop gain and bandwidth at high gain settings, as given by Equation 2. The second term in Equation 2 accounts for the division in feedback current that occurs between \( Z_i \) and \( R_f/R_g \) at the inverting node of the CLC400. This decrease in bandwidth can be circumvented as described in "Increasing Bandwidth at High Gains."

DC Accuracy and Noise

Since the two inputs for the CLC401 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. Specifically, the inverting input current noise is much larger than the non-inverting current noise. Also the two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting pin resistors ineffective.

In Equation 3, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaces the algebraic sum. \( R_s \) is the non-inverting pin resistance.

Equation 3

\[ V_O = \pm IBN x R_s (1 + R_f/R_g) \pm \frac{VIO (1 + R_f/R_g)}{1+R_f/R_g} \pm IBI x R_f \]

An important observation is that for fixed \( R_f \) offsets as referred to the input improve as the gain is increased (divide all terms by \( 1+R_f/R_g \)). A similar result is obtained for noise where noise figure improves as gain increases.
Selecting Between the CLC400 or CLC401

The CLC400 is intended for gains of ±1 to ±8 while the CLC401 is designed for gains of ±7 to ±50. Optimum performance is achieved with a feedback resistor of 250Ω with the CLC400 and 1.5Ω with the CLC401: this distinction may be important in transimpedance applications such as D/A buffering. Although the CLC400 can be used at higher gains, the CLC401 will provide a wider bandwidth because loop gain losses due to finite Zf are lower with the larger CLC401 feedback resistor as explained above. On the other hand, the lower recommended feedback resistance of the CLC400 minimizes the output errors due to inverting input noise and bias currents.

Increasing Bandwidth At High Gains

Bandwidth may be increased at high closed-loop gains by adjusting Rf and Rg to make up for the losses in loop gain that occur at these high gain settings due to current division at the inverting input. An approximate relationship may be obtained by holding the LG expression constant as the gain is changed from the design point used in the specifications (that is, Rf = 1.5kΩ and Rg = 79Ω). For the CLC401 this gives,

Equation 4

\[ R_f = 2500 \times 50A_v \quad \text{and} \quad R_g = \frac{2500 - 50A_v}{A_v - 1} \]

where \( A_v \) is the desired non-inverting gain. Note that with \( A_v = +20 \) we get the specified \( R_f = 1.5kΩ \). While at higher gains, a lower value gives stable performance with improved bandwidth.

Capacitive Feedback

Capacitive feedback should not be used with the CLC401 because of the potential for loop instability. See Application Note OA-7 for active filter realizations with the CLC401.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Parasitic or load capacitance directly on the output will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrate the required resistor value and resulting performance vs. capacitance.

Precision buffered resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with the slight decrease in bandwidth due to their reactive nature at high frequencies.

Evaluation PC boards (part no. CLC730013 for through-hole and CLC730027 for SOIC) for the CLC401 are available.
Physical Dimensions

inches (millimeters)

unless otherwise noted

8-Pin SOIC

NS Package Number M08A

8-Pin MDIP

NS Package Number N08E

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